External Reliability Evaluation Report

Qualification of subcontractor TSHT for products assembled in TSSOP8 package - GPA

General Information	
Product Line	0158, 0922, 3702
Product Description	Low power dual op-amps, Rail-to-rail dual op amp,
P/N	LM2904PT, TS922IPT, TS3702IPT
Product Group	AMS
Product division	GPA&RF
Package	TSSOP8
Silicon Process technology	Bipolar, HF2CMOS, HC1PA

Locations	
Wafer fab	Ang Mo Kio 6”
Assembly plant	TSHT (TianShui Huatian Technology) China
Reliability Lab	Grenoble

DOCUMENT INFORMATION

Version	Date	Pages	Comment
1.0	30-Aug-2019	12	First issue

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this evaluation is to qualify the subcontractor TSHT for the assembly of selected product in TSSOP8 package.
The line under qualification will serve several part numbers.
The qualification plan is based on the similarity and based on the JESD47 specification.
Here below are the details of the change depending on the affected product.

From ST Bouskoura to TSHT (see annex for product list)

Material	Current process	Modified process	Comment
Diffusion location	No change		
Assembly location	ST Bouskoura	TSHT	
Molding compound	Sumitomo G630AY	CEL-9220HF10	
Die attach	Ablestick 8601-S25	Henkel 8200T	
Lead-frame	Copper	Copper	
Wire	Copper 1 mil	Copper 1 mil Pd coated	
Plating	NiPdAgAu	Sn	
MSL	1	1	

3.2 Conclusion

Qualification Plan requirements will be fulfilled without exception. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Preliminary qualification results in line with expectation.

4 DEVICE CHARACTERISTICS

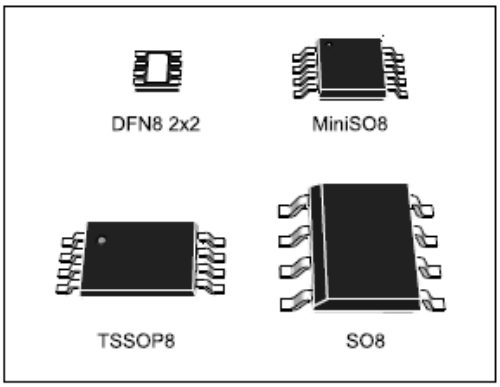
4.1 Device description

life.augmented

LM158, LM258, LM358

Low-power dual operational amplifiers

Datasheet - production data



Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current per channel essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to (V_{cc}^+ - 1.5 V)

Related products

- See LM158W for enhanced ESD ratings

Description

These circuits consist of two independent, high-gain, internally frequency-compensated op amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard 5 V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

This is information on a product in full production.

Reference: W836-TSHST TSSOP8-1

TS922, TS922A

Rail-to-rail, high output current, dual operational amplifier

Datasheet - production data

Flip-chip with backcoating

SO8

TSSOP8

Applications

- Headphone and servo amplifiers
- Sound cards, multimedia systems
- Line drivers, actuator drivers
- Mobile phones and portable equipment
- Instrumentation with low noise as key factor
- Piezoelectric speaker drivers

Description

TS922 and TS922A devices are rail-to-rail dual BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation. These devices have high output currents which allow low-load impedances to be driven.

Very low noise, low distortion, low offset, and a high output current capability make these devices an excellent choice for high quality, low voltage, or battery operated audio systems.

The devices are stable for capacitive loads up to 500 pF.

Features

- Rail-to-rail input and output
- Low noise: 9 nV/√Hz
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1 V/µs
- Operating from 2.7 to 12 V
- Low input offset voltage: 900 µV max. (TS922A)
- ESD internal protection: 2 kV
- Latch-up immunity
- Macromodel included in this specification
- Dual version available in Flip-chip package

TS3702

Micropower dual CMOS voltage comparators

Features

- Push-pull CMOS output (no external pull-up resistor required)
- Extremely low supply current: 9µA typ / comparator
- Wide single supply range: 2.7V to 16V or dual supplies (±1.35V to ±8V)
- Extremely low input bias current: 1pA typ
- Extremely low input offset currents: 1pA typ
- Input common-mode voltage range includes GND
- High input impedance: $10^{12}\Omega$ typ
- Fast response time: 2µs typ for 5mV overdrive
- Pin-to-pin and functionally compatible with bipolar LM393

Description

The TS3702 is a micropower CMOS dual voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

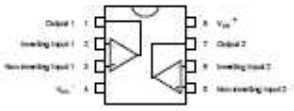
Thus response times remain similar to the LM393.

N
DIP8
(Plastic package)

D
SO8
(Plastic micropackage)

P
TSSOP8
(Thin shrink small outline package)

Pin connections
(Top view)



5 CONSTRUCTION NOTE

	New Plant Qualification			
	P/N LM358IPT	**PN/TS922IPT**	**PN/TS3702IPT**	
Wafer/Die fab. information				
Wafer fab manufacturing location	ST Singapore			
Technology	Bipolar	HF2CMOS	HC1PA	
Process family	Bipolar	BiCMOS2	CMOS	
Die finishing back side	Raw Silicon	Raw Silicon	Lapped silicon	
Die size	1070 x 1010 µm²	1720x1190µm²	1366x1136µm²	
Passivation type	SiN (nitride)	PVAPOX+Nitride	PVAPOX+Nitride	
Assembly information				
Assembly site	SC-Tianshui Huatian-China (TSHT)			
Package description	TSSOP8			
Molding compound	Hitachi CEL-9220HF10			
Frame material	Copper			
Die attach process	Glue			
Die attach material	Henkel 8200T-			
Wire bonding process	Wire			
Wires bonding materials/diameters	1.0mil PdCu			
Lead finishing process	Copper			
Lead finishing/bump solder material	Sn			
Final testing information				
Testing location	SC-Tianshui Huatian-China (TSHT) 999L			

6 TESTS RESULTS SUMMARY

6.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1				TSSOP8	0158	
2				TSSOP8	0922	
3				TSSOP8	3702	

Detailed results in below chapter will refer to P/N and Lot #.

6.2 Test plan and results summary

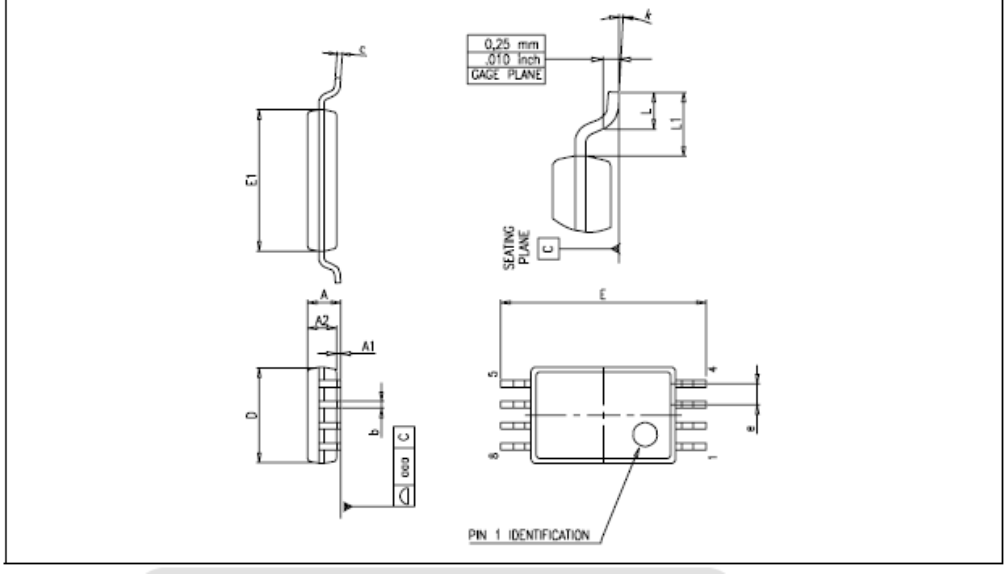
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1 0158	Lot 2 0922	Lot3 3702			
HTB/ HTOL	N	JESD22 A-108	Ta = 150°C, BIAS		168 H	78	0/78	0/78			
					500 H	78	0/78	0/78			
					1000 H	78	78	0/78			
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/78	0/78	0/78			
					500 H	0/78	78	0/78			
					1000 H	78	78	0/78			
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS			
UHAST	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/78	0/78	78			
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/78	0/78	78			
					500 cy	0/78	0/78	78			
					1000cy		0/78				
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	0/78	0/78	0/78			
					500 H	0/78	0/78	0/78			
					1000 H	78	78	78			

7 ANNEXES

7.1 Device details

7.1.1 Package outline/Mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	



7.1.2 Shear test results

Value in grams

	Ball Shear				Pull test			
	Max	Min	Average	Cpk	Max	Min	Average	Cpk
0158	43.33	38.72	40.76	3.02	15.72	12.15	14.19	2.77
0922	36.37	30.07	33.67	3.63	13.64	10.89	12.79	4.38
3702	34.42	32.38	33.4	2.61	14.46	12.11	13.23	3.43

7.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.